

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Use separate sheets as necessary)

2007

Complete if Known

Application Number	10/756,901
Filing Date	January 14, 2004
First Named Inventor	Farrar, Paul
Group Art Unit	2823
Examiner Name	Clark, Sheila

Sheet 1 of 1

Attorney Docket No: 303.572US2

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Filing Date If Appropriate

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	T ²

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
<i>ML</i>		BOHR, M. , "Interconnect scaling-the real limiter to high performance ULSI", International Electron Devices Meeting, IEEE, (1995),pp. 241-244	
<i>ML</i>		DAVIS, J. , et al., "A Priori Wiring Estimation and Optimal Multilevel Wiring Networks for Portable ULSI Systems", <u>Electronic Components and Technology Conference</u> , (1996),pp. 1002-1008	
<i>ML</i>		GWENNAP, L. , "IC Makers Confront RC Limitations", <u>Microdesign Resources</u> , Microprocessor Report,(1997),pp. 14-18	
<i>ML</i>		KANTA, C. , et al., "Dual Damascene: A ULSI Wiring Technology", <u>VMIC Conference</u> , (1991),pp. 144-152	
<i>ML</i>		LAKSHMINARAYANAN, S. , Multilevel Dual Damascene Copper Interconnections, Rensselaer Polytechnic Institute, Ph.D Thesis,(1997),1-205	
<i>ML</i>		LICATA, T. , et al., "Dual Damascene Al Wiring for 256M DRAM", Proceedings of the 12th International VLSI Multilevel Interconnection Conference, (1995),pp. 596-602	
<i>ML</i>		LUTHER, B. , et al., "Planar Copper-Polyimide Back End of the Line Interconnections for ULSI Devices", VMIC Conference, (1993),pp. 15-21	
<i>ML</i>		RYAN, J. , et al., "The evolution of interconnection technology at IBM", IBM J. Res. Develop., 39(4), (1995),pp. 371-381	
<i>ML</i>		SINGER, P. , "New Interconnect Materials: Chasing the Promise of Faster Chips", Semiconductor International, (1994),pp. 52-56	
<i>ML</i>		TAUR, Y. , "CMOS scaling into the 21st century: 0.1 micrometer and beyond", IBM J. Res. Develop., 39(1/2), (1995),pp. 245-260	
<i>ML</i>		VOLLMER, B. , et al., "Recent advances in the application of collimated sputtering", Thin Solid Films, 247, (1994),pp. 104-111	

EXAMINER

DATE CONSIDERED

2/19/01

Substitute Disclosure Statement Form (PTO-1449)

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